1st Sem D.E

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12EC021

M.Tech. Degree Examination, June/July 2014
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain DC characteristics of CMOS inverter. **(10 Marks)**

b. With a neat circuit describe body effect. **(05 Marks)**

c. Calculate the native threshold voltage for an n-transistor at 300°K for a process with Si-substrate with $N_A = 1.80 \times 10^{16}$ cm^{-3}, a S_iO_2 gate oxide with thickness 200°A. (Assume $\phi ms = -0.9V$, $Qf_c = 0.0$, $N_i = 1.45 \times 10^{10}$ cm^{-3} at 300°K, $K = 1.380 \times 10^{-23}$ J/°K, $q = 1.602 \times 10^{-19}$C and $Es_i = 1.06 \times 10^{-12}$ F/cm). **(05 Marks)**

2 a. Describe the channel length modulation, drain punch through and impact ionization effects. **(06 Marks)**

b. Describe the transmission gate characteristics for control input changing and for switched input changing. **(08 Marks)**

c. Explain the working of basic Bi-CMOS inverter. **(06 Marks)**

3 a. Explain λ-based design rules for wires, transistors and contacts of nMOS and CMOS circuits. **(10 Marks)**

b. Two nMOS inverters are cascaded to drive a capacitive load C_L = 16 □ Cg as shown in Fig.Q.3(a). Calculate the pair delay (V_{in} to V_{out}) for inverter geometry shown in Fig.Q.3(a). What are the ratios of each inverters? If strays and wirings are allowed for it would be reasonable to increase capacitance to ground across the output of each inverter by 4 □ Cg. What is pair delay allowing for strays? Assume (5 = 0.3 nsec for 5μm MOS technology). **(10 Marks)**

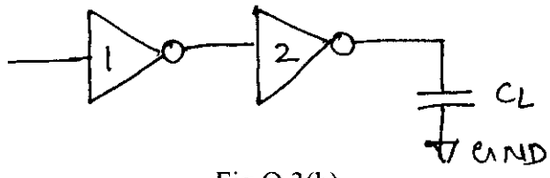

Fig.Q.3(b)

Inverter 1	Inverter 2
$L_{pu} = 16\lambda$	$L_{pu} = 2\lambda$
$W_{pu} = 2\lambda$	$W_{pu} = 2\lambda$
$L_{pd} = 2\lambda$	$L_{pd} = 2\lambda$
$W_{pd} = 2\lambda$	$W_{pd} = 8\lambda$

4 a. Draw the schematic and stick diagram for the following:

i) nMOS inverter ii) $Y = \overline{AB + C}$ using CMOS logic. **(06 Marks)**

b. With neat sketches, explain the fabrication of CMOS inverter using P-well process. **(08 Marks)**

c. Explain Latch-up problem in pwell structure. **(06 Marks)**

5 a. Obtain the scaling factors for the following:
   i) Channel resistance (Ron).
   ii) Maximum operating frequency (fo).
   iii) Power dissipation per unit are (Pa). **(03 Marks)**
   b. Design 4:1 MUX using transmission gates. **(07 Marks)**
   c. Draw the stick diagram and layout for the expression Z = A(D + E) + BC. Using CMOS logic. **(10 Marks)**

6 a. Explain the working of CMOS SR latch circuit based on NOR2 gates. **(06 Marks)**
   b. Explain the principle of pass transistor logic and derive equation $V_x(t)$ for logic "1" transfer. **(08 Marks)**
   c. With a neat circuit diagram, describe voltage bootstrapping. **(06 Marks)**

7 a. Describe the working of ratio less dynamic shift register. **(06 Marks)**
   b. What are the limitations associated with domino CMOS logic? Describe the remedial methods to overcome these problems. **(10 Marks)**
   c. List the advantages of CMOS over NMOS. **(04 Marks)**

8 a. Describe the clock generation and clock distribution schemes. **(10 Marks)**
   b. With a neat circuit diagram, explain the common source stage with resistive load. Derive the small signal voltage gain for the same. **(10 Marks)**

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